

SHARP SERVICE MANUAL

CODE:00ZMZ800OPT/E

MZ-800SERIES OPTION

FLOPPY DISK DRIVE	MZ-1F19
MZ DISK INTERFACE	MZ-1E19
RAM FILE	MZ-1R18
OPTION RAM	MZ-1R25
DATA RECORDER	MZ-1T04

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1. MZ-1F19
2. MZ-1E19
3. MZ-1R18

PARTS GUIDE & LIST

(FOR MZ-R25 AND MZ1T04ARE PARTS LIST ONLY)

1. MZ-1F19

1-1. Specification

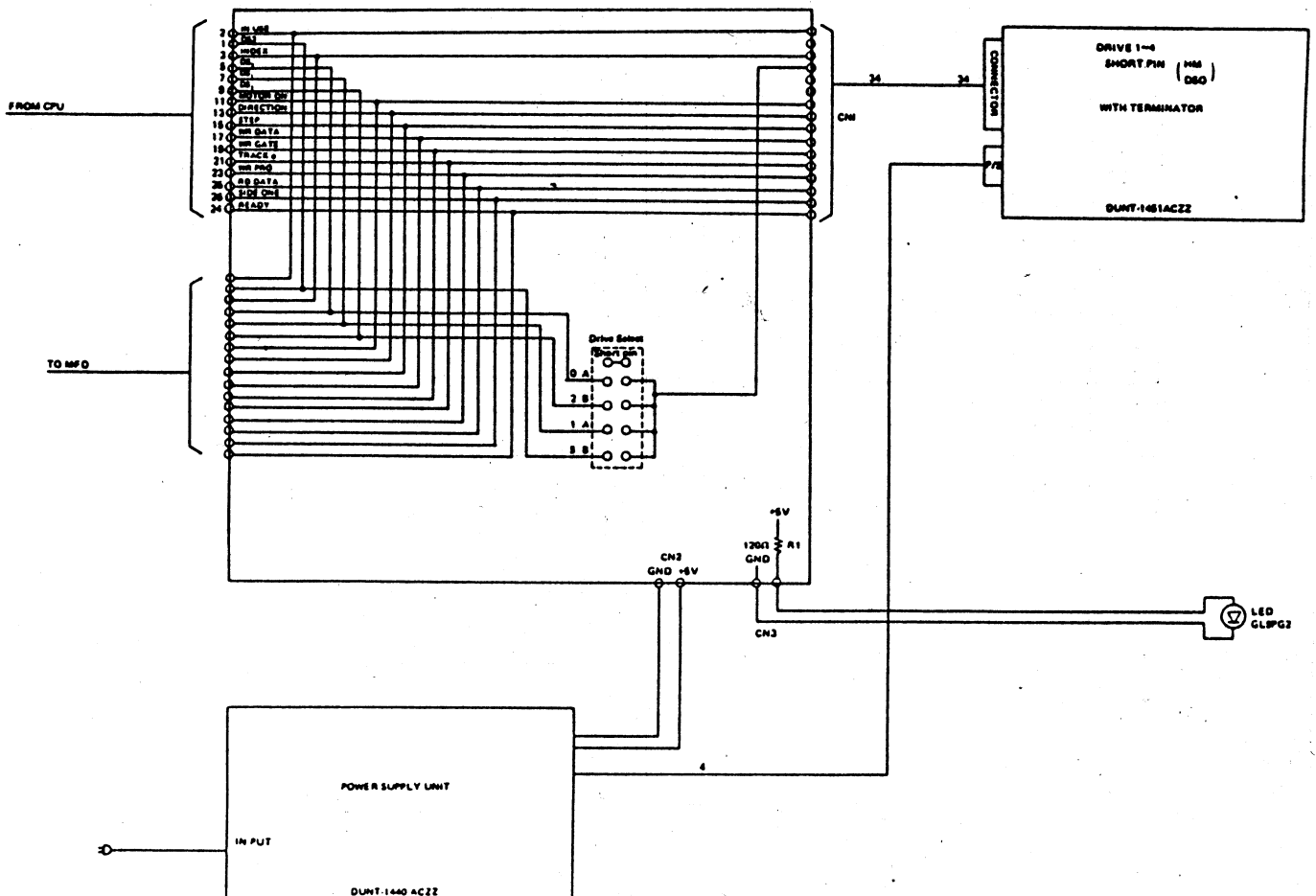
Outline

The MZ-1F19 is an mini-floppy disk unit designed for use with the MZ-800 Series Personal Computer. The unit should be use with the MZ-1E05 I/F PWB unit.

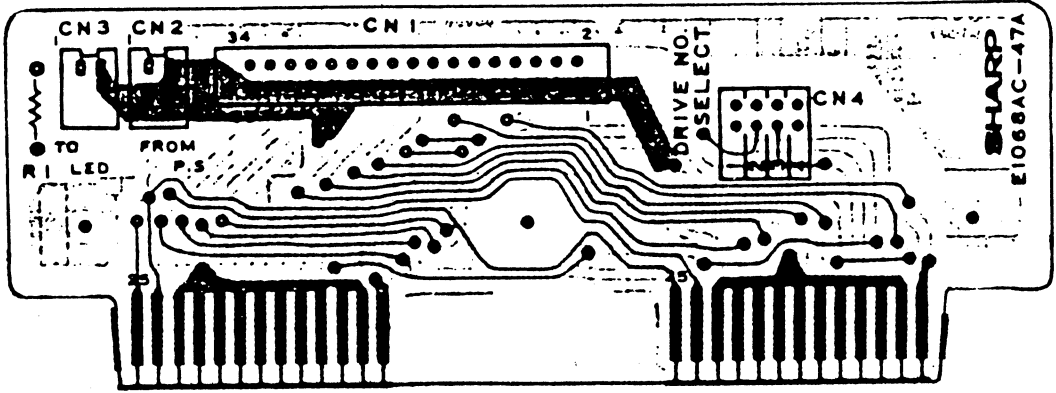
Specification

Model name : MZ-1F19
 Recording capacity : 320K
 Tracks : 40 tracks
 Sectors : 16 sector
 Recording medium : 5-1/4" disk
 Power supply : 220V/240V 50/60Hz
 Power consumption : 20W
 Operating temperature : 10°C to 35°C
 Operating humidity : 20% to 80%RH, w/o moisture condensation
 Physical dimensions : 118(W) x 331(D) x 189(H) mm
 Weight : 5.1 Kg
 Accessories : Instruction book, drive number label, power cord.

1-2. System Block Diagram



1-3. Signal Position of Connector (SUB PWB)

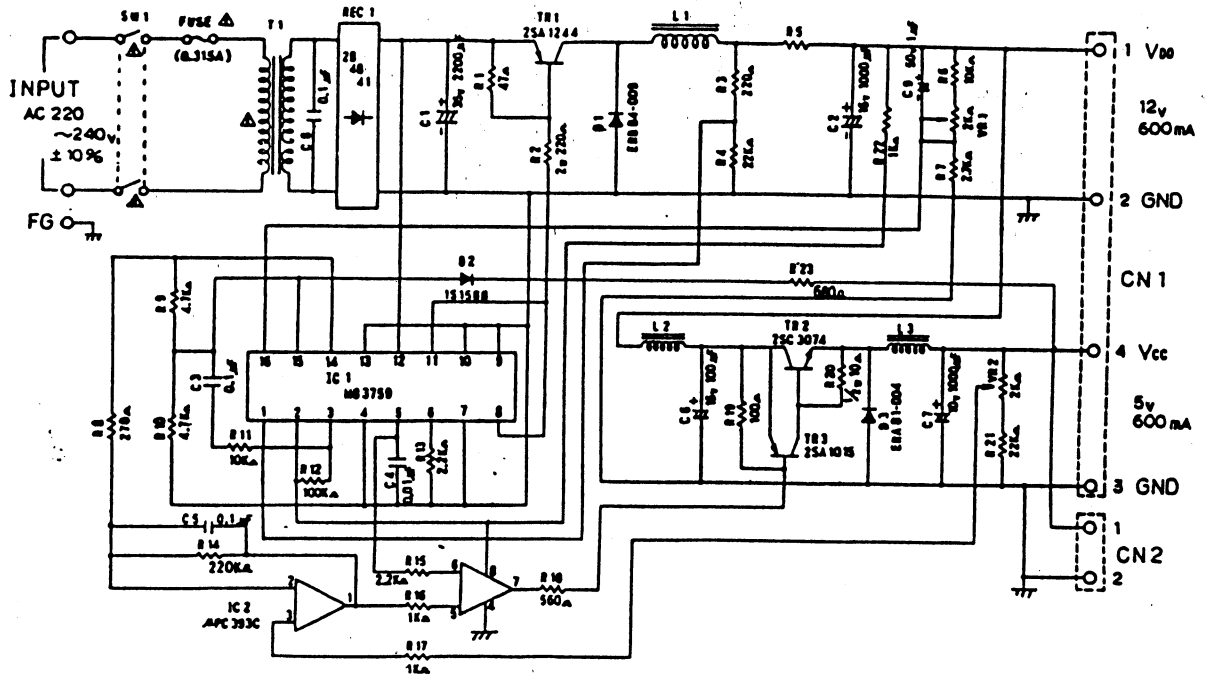


(From CPU
To IF19)

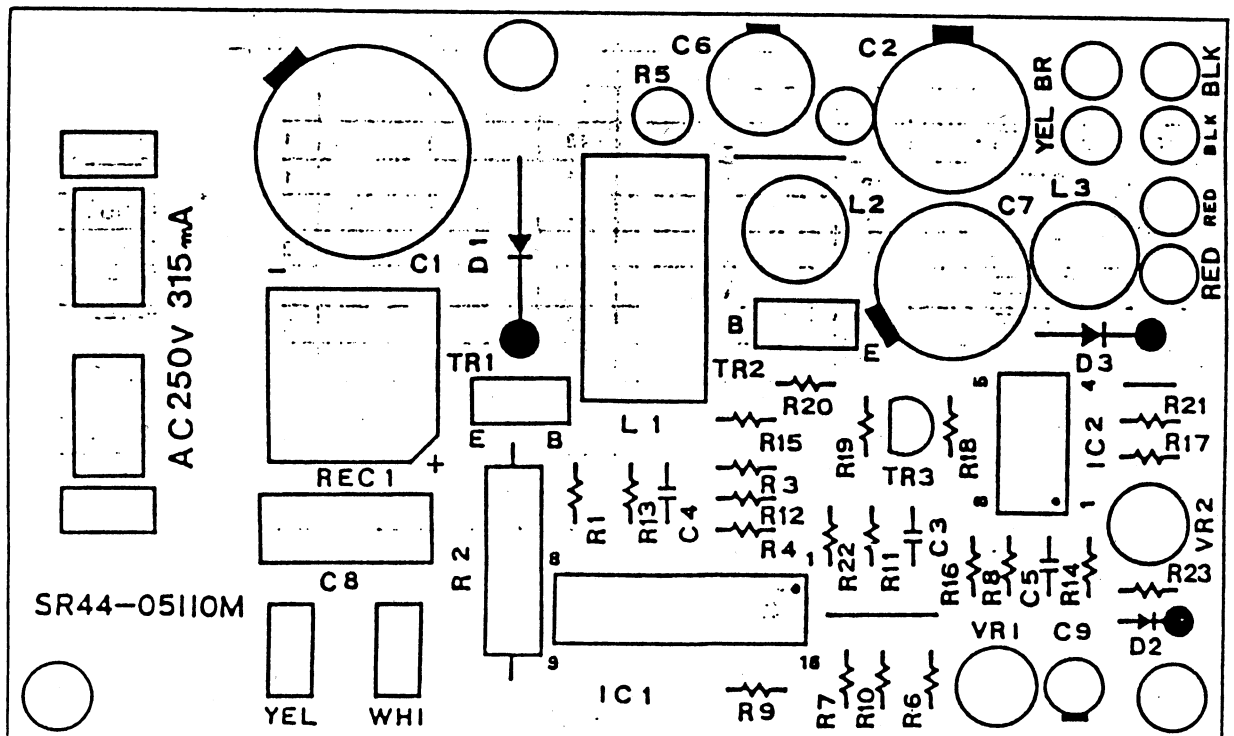
MFD (To FD 54B)

No	Signal Name	No	Signal Name	No	Signal Name	No	Signal Name	
1	SEL 3	2	IN USE	1	↑	2	IN USE	
3	INDEX	4	↑	3		4	IN USE	
5	SEL 0	6		↑		5	6	IN USE
7	SEL 1	8	7			8	INDEX	
9	SEL 2	10	9			10	SEL 0	
11	MOTOR ON	12	GND	11		↑	12	IN USE
13	DIRECTION	14		13			14	IN USE
15	STEP	16		15			16	MOTOR ON
17	WR DATA	18		17			18	DIRECTION
19	WR GATE	20	GND	19			↑	20
21	TRACK 0	22		21	22			WR DATA
23	WR PRO	24	REDY	23	24			WR GATE
25	RD DATA	26	SIDE	25	26			TRACK 0
				27	28			WR PRO
				29	30			RD DATA
				31	32	SIDE		
				33	34	REDY		

1-4. Power Supply Circuit Diagram



Power Supply Lay Out



2. MZ-1E19

2-1. General

The MZ-1E19 is the MZ disk interfacing board designed for use with the MZ-800.

2-2. Function

As the MZ-1F11 is connected with the MZ-800 series, it drives the MZ disk.

2-3. Connection method

Remove the cassette tape of the MZ-800 and install the MZ-1F11 together with the louver cover. Install the MZ-1E19 in the MZ-800 slot or the MZ-1U06 expansion unit. Fasten the cable extended from the rear part of the MZ-1F11 with the MZ-1E19.

2-4. Specification

Operating voltage: 5V DC \pm 5%

IC used: LS00, LS02, LS244

Physical dimensions: 116(W) x 144(D) x 19(H) mm

2-5. Buffer

The following signals go through the SNLS244 buffer. $\overline{\text{IORW}}$, RESET, RD, CE, S1, S0, ϕ , $\overline{\text{M1}}$

2-6. Function

I/O selector:

When the CPU accesses I/O address of the MZ disk, it enables SIO of the MZ-1F11.

I/O port	CE	S1	S2	SIO register
\$F4	0	0	0	Ch A data
\$F5	0	0	1	Ch B data
\$F6	0	1	0	Ch A CWR
\$F7	0	1	1	Ch B CWR

Table 2-1

CE: MZ-1F11 SIO chip enable

S1: MZ-1F11 SIO control/data select

S0: MZ-1F11 SIO B/A channel select

2-7. MZ-1E19 timings

Because the MZ-1E19 is connected to the SIO on the MZ-1F11 board, timings are identical to those of the SIO.

When the CPU sends data on the I/O address port F4H ~ F7H, the chip enable CE is turned low level (active) and write or read will be conducted in the following timings.

(1) Read cycle

Shown next is the timings to read Z-80 SIO data or status register. Z-80 CPU input command can be used to read data or status.

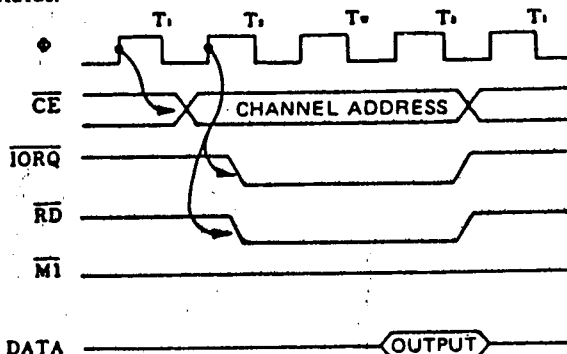


Fig. 2-1 Read cycle

(2) Write cycle

Shown next is the timings to write the Z-80 SIO or control word. Z-80 CPU output command can be used to write data or control word.

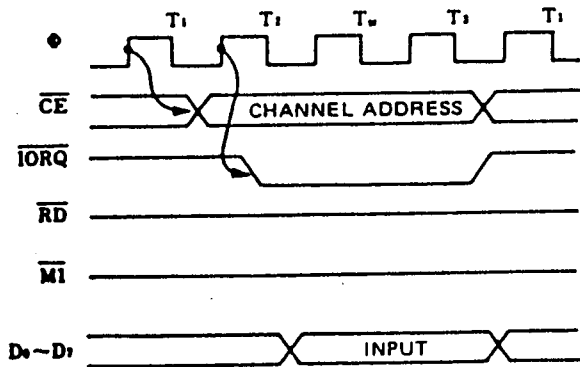


Fig. 2-2 Write cycle

2-8. Troubleshooting

As I/O address is selected as described in the paragraph discussing function, the MZ-1E19 will be operating normally if signals in the table above should be on \$F4 ~ \$F7.

Check method

Tools required: MZ-800

Oscilloscope

Procedure

1. Start the MZ-800 monitor and enter the sample program (below).
2. Start the program and observe waveforms of CE, S0 and S1 on the oscilloscope (NOTE).
3. Repeat the above two steps for each of \$F4 through \$F7 to check if they are as described in the table.

NOTE: Because port is selected by a pulse signal, all CE, S1, and S0 are in a pulse form.

Sample program

```
B1: LD A, 00H      3E00
    LD (F4H), A   D3F4
    JR B1         18FA
```

Changing F4 to F4 through F7, you will be able to check all ports.

*M2000

2000 00 3E : Practical example from address 2000

2001 00 00

2002 00 D3

2003 00 F4

2004 00 18

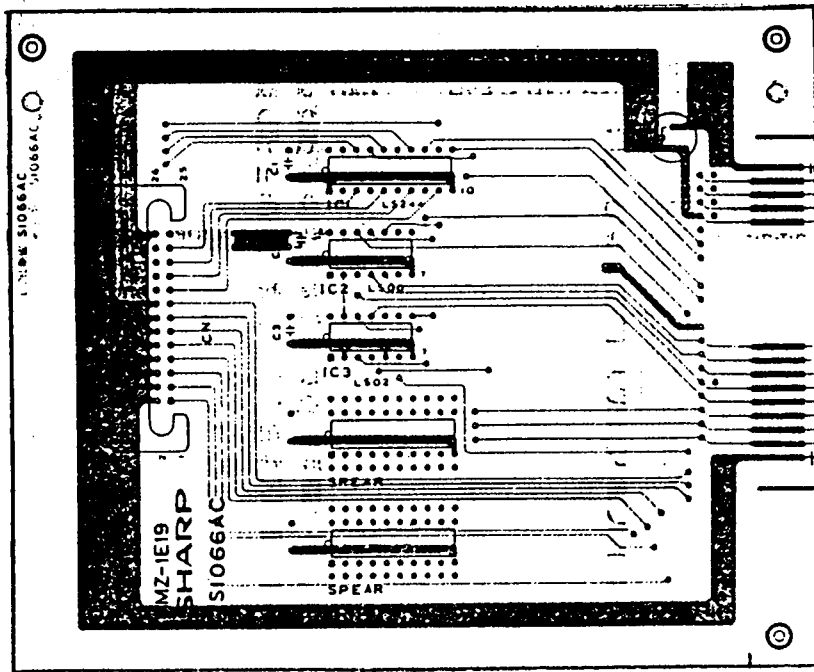
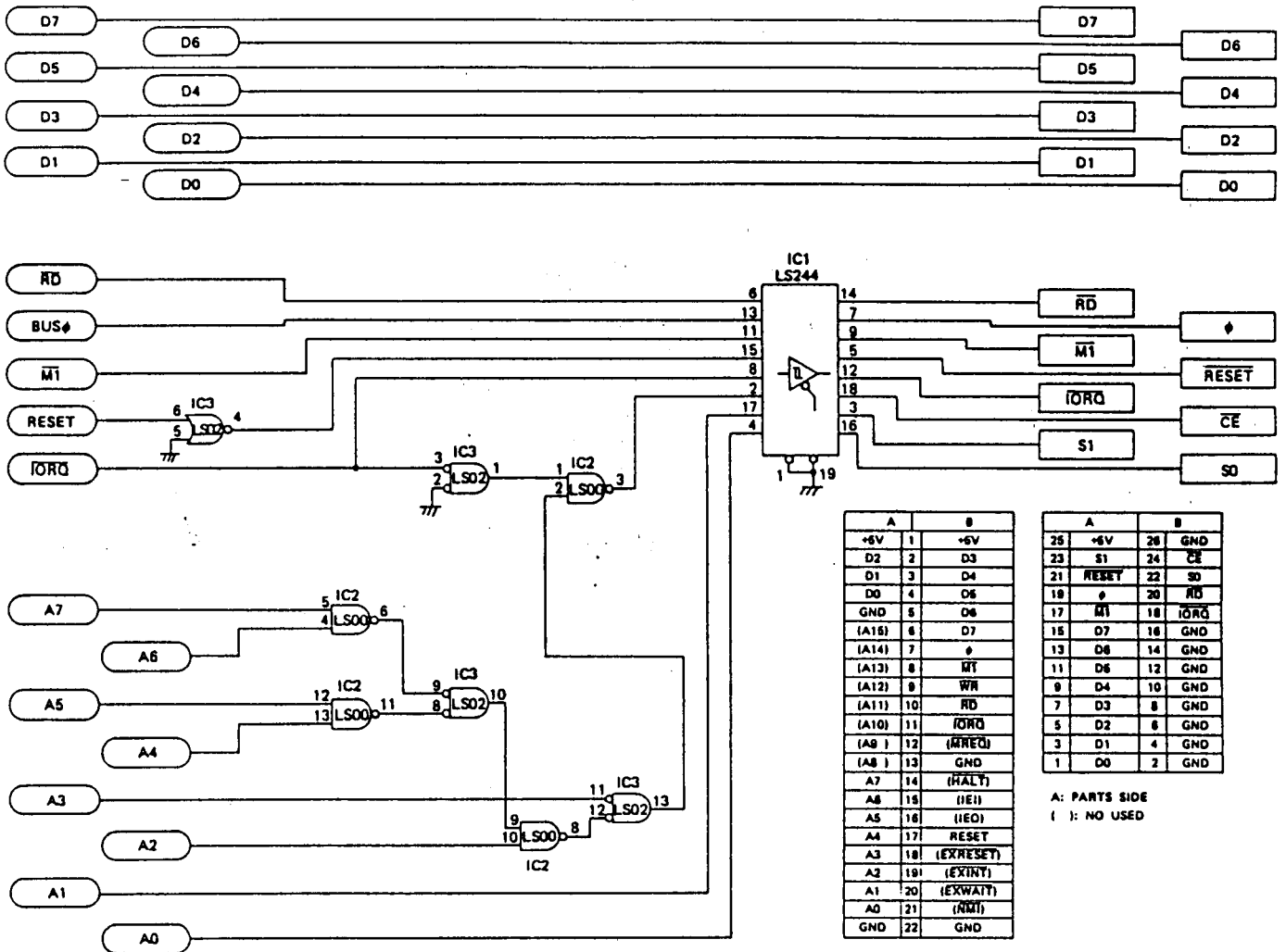
2005 00 FA

Address 2003 is tried to change from F4H to F7H.

Trouble phenomenon and cause (provided that QD is normal)

- QD does not appear in the menu at power on to the MZ-800.
 - Loose connector
 - CE not on
- UNFORMAT error occurs at all times even if the media has been written.
 - Open in the address line of S1 or A1
 - LS244 failure
- MAKE READY QD is displayed even if the media was set.
 - Open in the address line of S0 or A0
 - Failure in LS244
- Reset not done
- Failure in LS02 or LS244

2.9. Circuit diagram



30 Ram

3. MZ-1R18 (RAM file)

3-1. MZ-1R18 is the 64KB RAM file for use with the MZ-800 which is housed in the I/O slot.

The RAM file is used as an external memory unit. It can be used same as the floppy disk and cassette tape. But, the memory contents will be deleted when power is turned off. It can be used for fast data write and read in the program.

3-2. Specification

RAM	64KB ... M5K4164P-20 equivalent x 8 Read, write, and address automatic increment functions
	Housed in the MZ-800 I/O slot I/O address EA, EB fixed EA ... Data EB ... Address

3-3. Installation method (subject to change without notice)

Observe the following method to install the RAM file. Remove three screws in the rear part of the MZ-800 which are not on the data recorder side, and remove the cabinet from the MZ-800. As the connector comes unfastened as in Fig. 3, it should be fastened again.

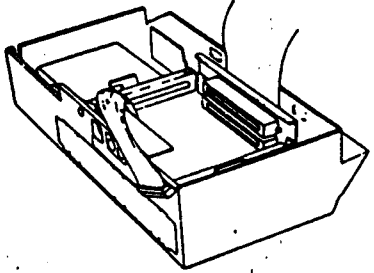


Fig. 1

Place the cabinet upside down and engage the RAM file to the connector in a manner as illustrated. The latch at the rear of the RAM file should be engaged perfectly.

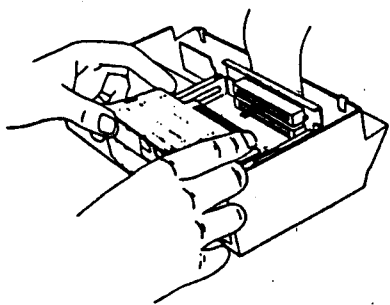


Fig. 2

As connectors at (1) and (2) come disengaged when the cabinet is removed, they should be fastened again as before. When the RAM file has been complete to install, replace the cabinet back on its position.

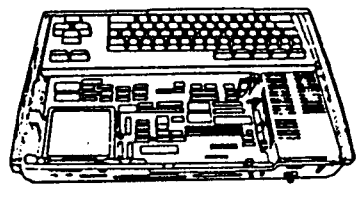


Fig. 3

3-4. Use (software)

With the MZ-800 BASIC, it supports commands such as INIT, LOADALL, SAVEALL. For more details, refer to the MZ-800 BASIC Programming Manual.

3-5. Use by the machine language

Address assigned to the MZ-1R18 ... I/O address EBH
Data write to MZ-1R18 ... I/O address EAH

1) Write sequence

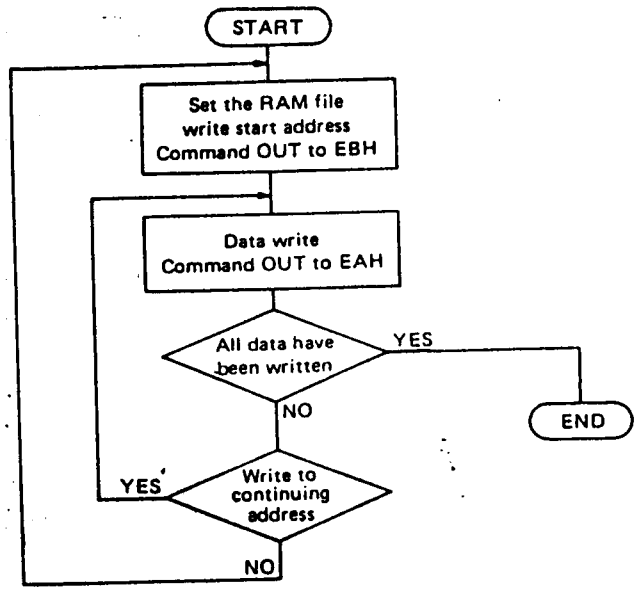


Fig. 4

[Example-1] Data "\$41" is written in the RAM file address \$D3C5.

LD A, C5H ... low order address of the RAM file
LD B, D3H ... high order address of the RAM file
LD C, EBH ... I/O address
OUT (C), A ... Use the indirect OUT.
LA A, 41H
OUT (EAH), A

Address setup	3E C5
	06 D3
	0E EB
	ED 49
	3E 41
	D3 EA

Use the indirect OUT command for address assignment.

2) Read sequence

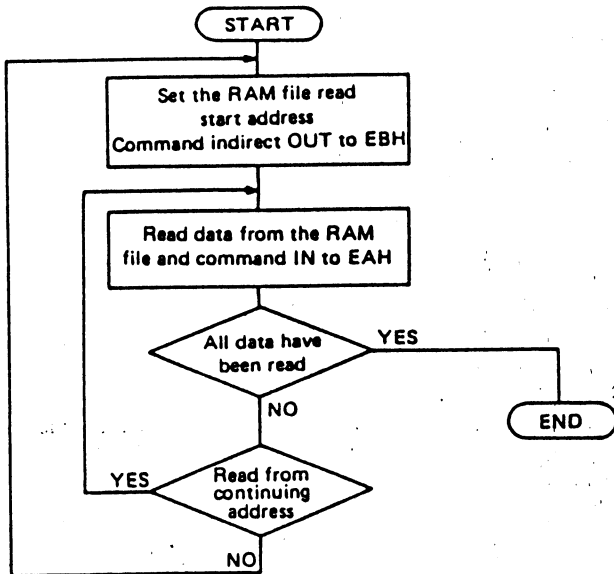


Fig. 5

[Example-2] Data in the RAM file address SCD01 are read and transferred to the register A.

LD A, 01H ... low order address of the RAM file
 LD B, CDH ... high order address of the RAM file
 LD C, EBH ... I/O address
 OUT (C), A
 IN A, (EAH)

Address setup

3E	01
06	CD
0E	EB
ED	49
DB	EA

3-6. Block diagram

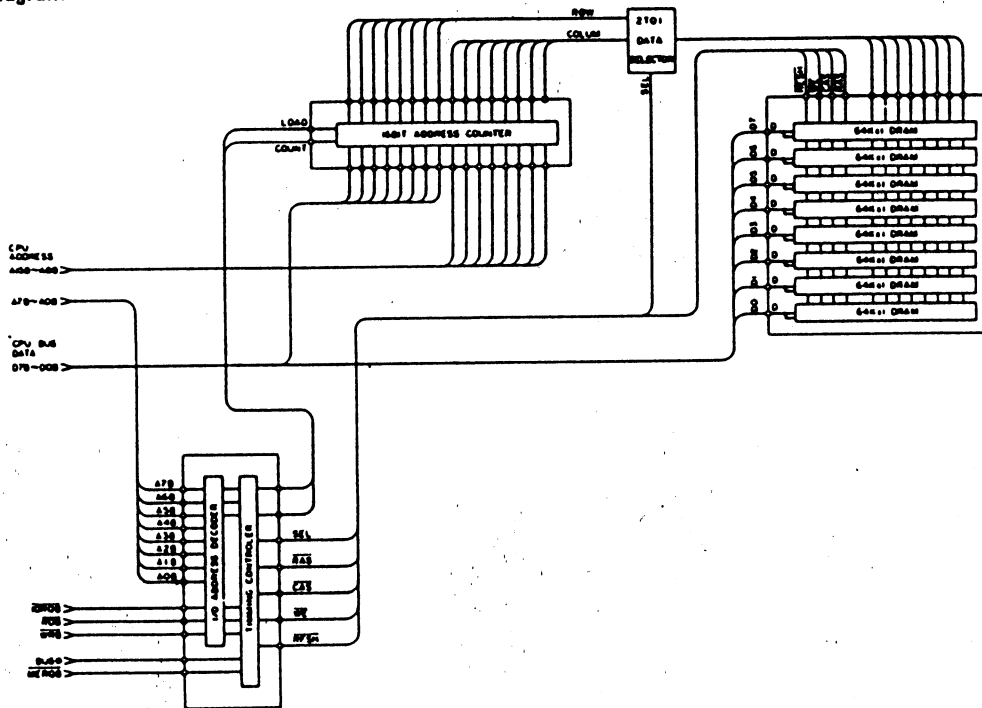


Fig. 6

3-6-1. I/O address decoder

The I/O address decoder determines the I/O address of this card and it had been set to 0EAH and 0EBH (\$EA, \$EB) for the MZ-1R18.

3-6-2. DRAM

It comprises the 64KB memory capacity by using 8 chips of 64KB x 1 RAM. As the RAM has the refresh line, attention must be paid when replacing it.

3-6-3. Timing controller

Generates the signal required for DRAM read and write.

\overline{RAS} ... DRAM row address strobe

\overline{CAS} ... DRAM column address strobe

SEL ... Row address and column address multiplexing signal

\overline{WE} ... DRAM write enable

\overline{RFSH} ... DRAM refresh signal. Refresh is carried out in synchronization with \overline{IMERW} of the CPU.

LOAD ... DRAM address is set in the address counter.
COUNT ... Issued each time data are written or read to/from the DRAM which is used to increment the address counter.

3-6-5. 2-to-1 data selector

Output from the 16-bit address counter is multiplexed to create the DRAM row and column addresses.

3-6-4. 16-bit address counter

Preset enabled 16 bits long counter from which the DRAM address is generated. It is used for the automatic increment function.

3-7. Timings

3-7-1. RAM file address address assignment

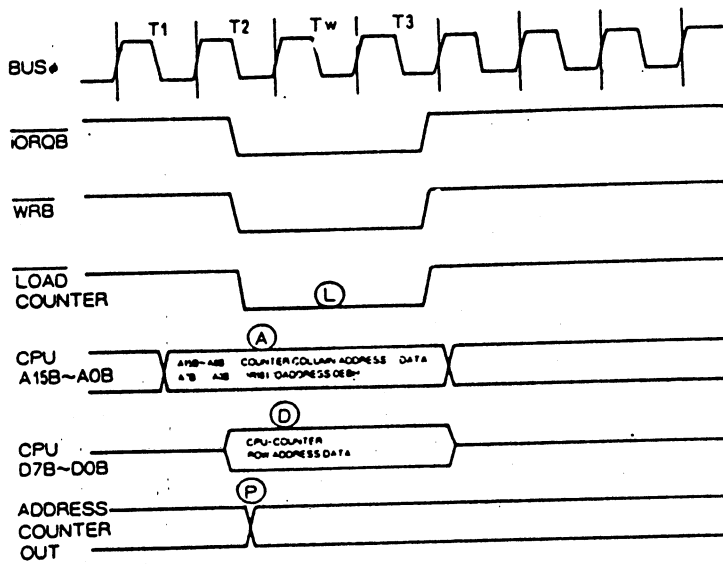


Fig. 7

Explanation) A 16-bit initial address is set in the 16-bit address counter.

- o I/O address SEA (0EAH) of the address counter is output to the CPU address bus A7 - A0. (A)
- o Next, \overline{IORQB} , \overline{WRB} from the CPU, turned low, which causes \overline{LOAD} to go low. (L)

- o At this point, high order 8 bits of the data to be set in the counter are output to A15B ~ A8B and low order 8 bits of the data to be set in the counter are output from the CPU to D7B ~ D0B. (A), (D)
- o When \overline{LOAD} goes low, A15B ~ A8B and D7B~D0B from the CPU are set in the counter. (P)

3-7-2. Data write to DRAM

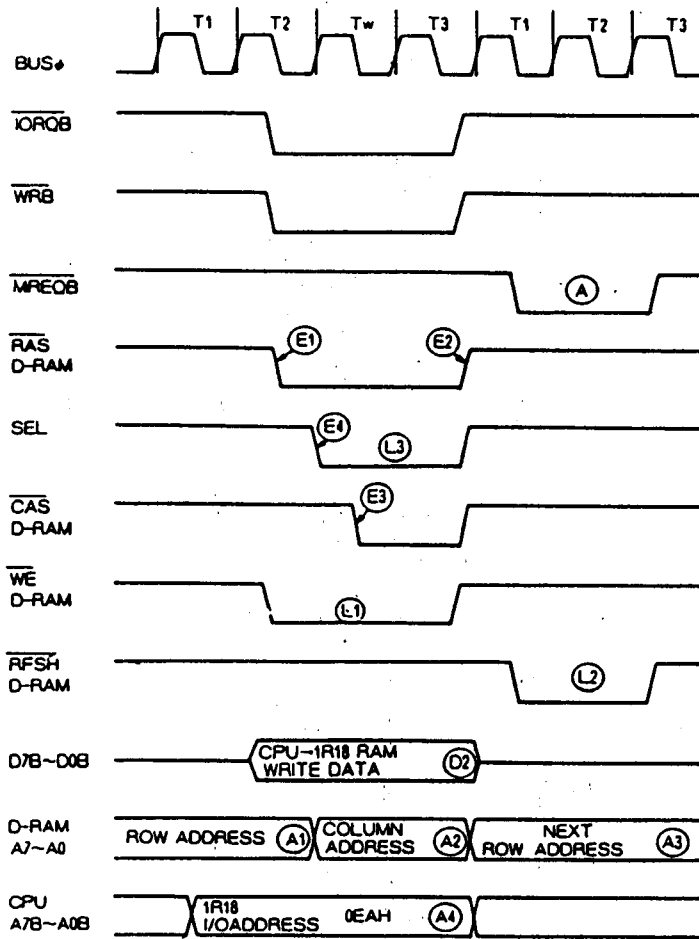


Fig. 8

Explanation)

- (1) When data are output on the DRAM data input port \overline{SEB} (0EBH), it makes \overline{IORQ} and \overline{WRB} turned low.
- (2) This makes DRAM \overline{RAS} forced low level. At a falling edge of RAM, low order 8 bits in the address counter are read as the DRAM row address. (E1)
- (3) Next, \overline{RAS} is sampled at a rising edge of \overline{RAS} to create SEL. (E4)
SEL signal is connected to select line of the 2-to-1 data selector. When SEL is low, the DRAM row address (high order 8 bits of the address counter) is given.
- (4) \overline{CAS} is created by sampling SEL signal at a falling edge of TW. (E3)
DRAM reads high order 8 bits in the address counter as the DRAM custom address at a falling edge of \overline{CAS} . Because DRAM \overline{WE} is in a low level at this stage (L1), it results in early write (see NOTE), data in D7B ~ D0B are written in the RAM.
- (5) When \overline{IORQ} or \overline{WR} changes from low to high level, it forces \overline{RAS} , \overline{CAS} , and SEL high level, so as to terminate RAM accessing.

The address counter is counted up at a low to high transition of \overline{RAS} . (E2)

- (6) \overline{RFSH} goes low in synchronization with \overline{MREQ} and refreshes the DRAM. (L2)

NOTE: Early write

For the DRAM write cycle, there are late write cycle during which \overline{WE} is set low after making \overline{CAS} turned low and the early write cycle during which \overline{WE} is forced low and \overline{CAS} is forced low.

Major difference of these two is that the data in the assigned address are output to the output pin in the late write cycle and that output pin is kept in high impedance in the early write cycle.

When the output pin is in high impedance, bus can be shared common by connecting input pin with output pin.

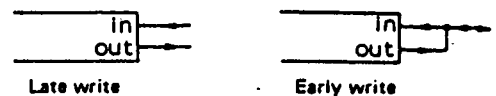


Fig. 9

3-7-3. Read from the DRAM

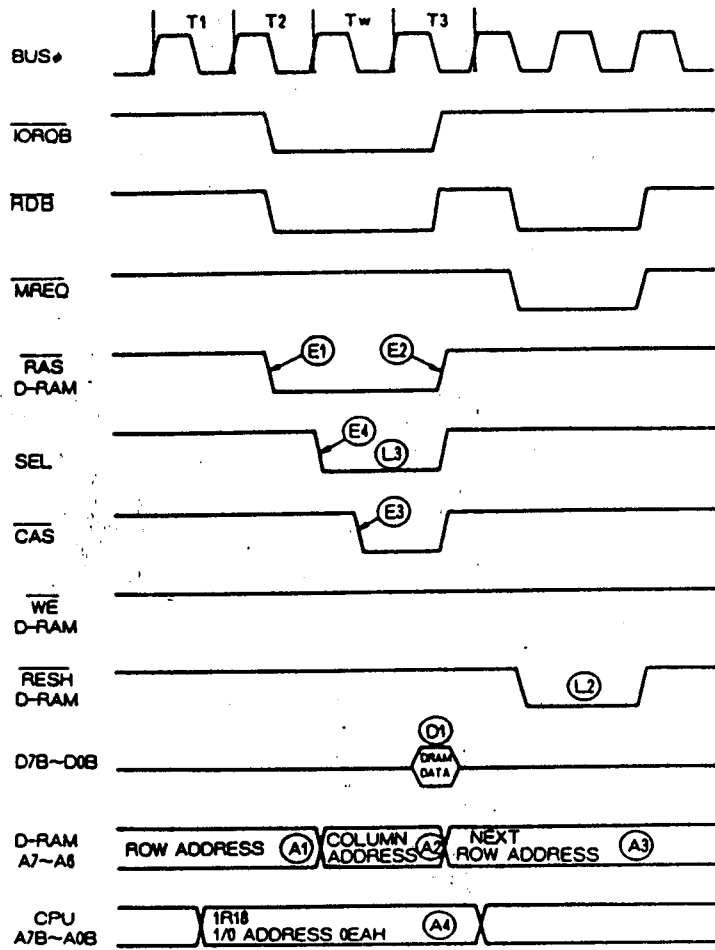


Fig. 10

Explanation)

- (1) When an input command is executed to the DRAM data I/O port SEB (0EBH), it makes $\overline{\text{IORQB}}$ and $\overline{\text{RDB}}$ turned low level.
- (2) This makes the DRAM RAS forced low. At this falling edge, low order 8 bits in the address counter are read as the DRAM row address. (E1)
- (3) SEL signal is used to multiplex the address counter 16 bits into two parts of eight bits each. (L3) (A2)
This signal can be obtained by sampling $\overline{\text{RAS}}$ at a rising edge of Tw. (E4)
- (4) $\overline{\text{CAS}}$ is obtained by sampling SEL signal at a falling edge of Tw.
High order 8 bits in the address counter that multiplexed by a falling edge of $\overline{\text{CAS}}$ are read by the DRAM as a column address. (E3)
- (5) After a certain time (access time) from a falling edge of $\overline{\text{CAS}}$, valid data, D7B~D0B, are sent from the DRAM. (D1)
- (6) The CPU read the data on the data bus at a falling edge of T3. (D1).
- (7) When $\overline{\text{IORQB}}$ or $\overline{\text{RDB}}$ changes from low to high level, it forces $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and SEL high and the DRAM accessing terminates.
- (8) At a low to high transition of $\overline{\text{RAS}}$, the address counter is counter up. (E2)

1 MZ1F19 Exteriors

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	DUNTK1438ACZZ	BE	N	E	Sub PWB unit
2	DUNTK1439ACZZ	AK		E	LED PWB unit
3	GFTAR1014ACZZ	AC		D	Lid for connector
4	LANGK1012ACZZ	AK		D	Angle for PWB
5	LHLDW2008SCZZ	AB		D	Mini clamp S-5 (S-5)
6	PSPAX1005ACZZ	AF		C	Spacer for PWB
7	DUNT-1451ACZZ	**	N	E	Drive unit
8	GFTAF1002ACZZ	AE		D	Cover (Single drive type)
9	GCABC1010ACZZ	AQ		D	Front panel
10	CCAB-1009ACZZ	BD		C	Cabinet unit (rear)
11	LCHSM1019ACZZ	AW	N	C	Chassis
12	HBDGB3002GES	AE		D	SHARP Badge
13	GLEGP0010UCZZ	AB		C	Rubber foot
14	GFTAS1013ACZZ	AF		D	Lid
15	XBPSD30P08KS0	AA		C	Screw (3x8KS)
16	XBPSD30P18KS0	AA		C	Screw
17	XBPSD40P06K00	AA		B	Screw (4x6K)
18	XUPSD30P06000	AA		C	Screw (3x6)
19	XBPSD30P06KS0	AA		C	Screw (3x6KS)
20	XBSSD30P06000	AA		B	Screw (3x6)
21	XBPSD30P06K00	AA		C	Screw (3x6K)
22	XBBSC30P06000	AA		C	Screw (3x6)
23	XWHNZ30-05080	AA		C	Washer (3φ)
24	XBTSC30P06000	AA		C	Screw (3x6)
25	LBNDJ0004UCZZ	AA		C	Binl-tye (for Ring core)
26	DUNT-1440ACZZ	BR		E	Power supply unit

2 MZ1F19 Electronic parts

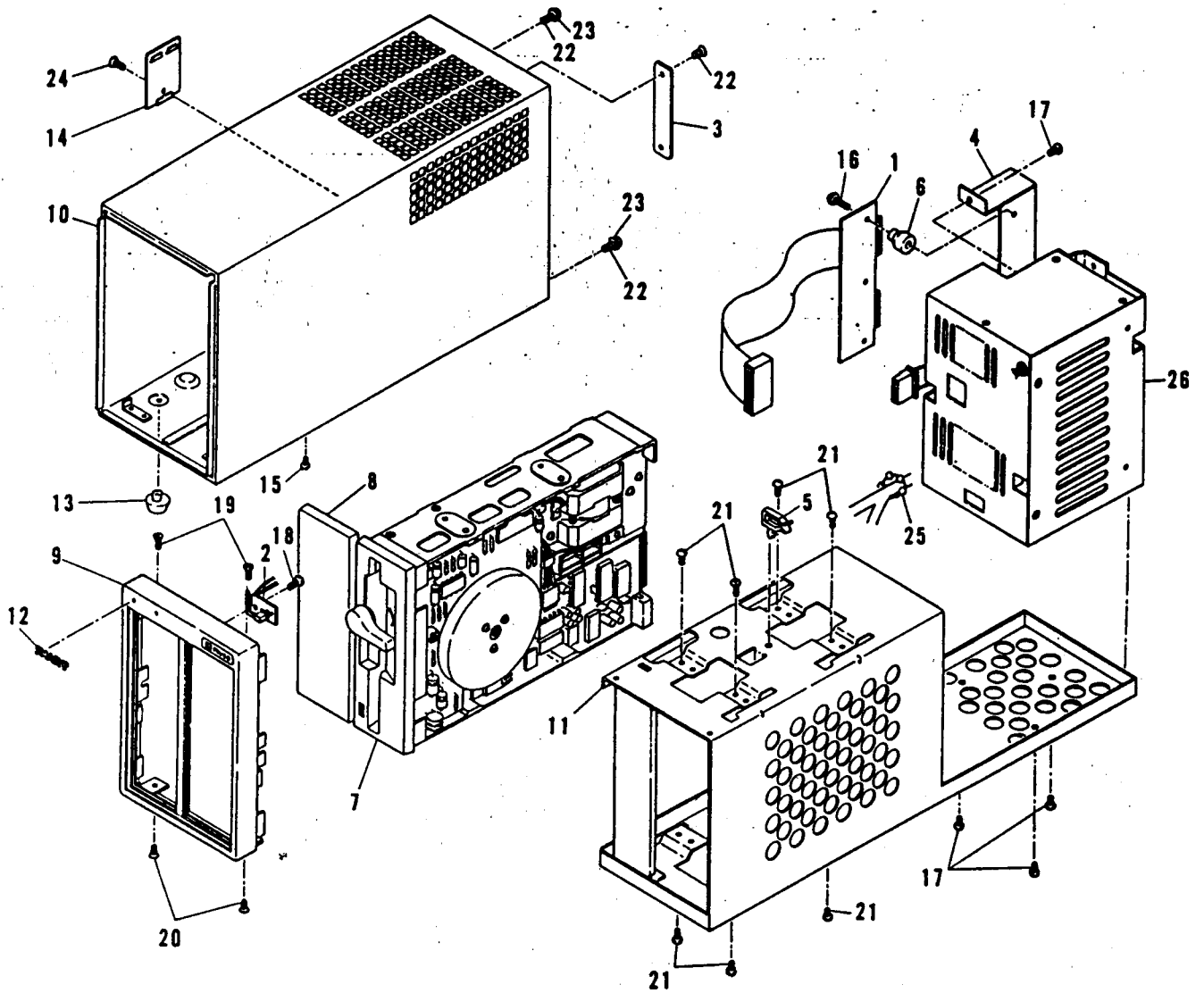
NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	QACCE3620QCZZ	AL		C	AC cord
2	QCNCM1015ACZZ	AC		B	Connector (2pin)
3	QCNCM1058AC08	AB		C	Connector
4	QCNCW1057ACZZ	AB		C	Connector
5	QCNW-1113ACZZ	AW		C	FD connector cable
6	QCNW-1114ACZZ	AC		C	2p LED harness
7	VHPGL9PG2//--1	AC		B	LED (GL9PG2)
8	VRD-ST2EY121J	AA		C	Resistor (1/4W 120Ω ±5%)

3 MZ1F19 Packing & Others

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	SPAKA1009ACZZ	AB		D	Cord sleeve
2	SPAKA1114ACZZ	AV		D	Packing cushion
3	SPAKC1607ACZZ	AR	N	D	Packing case
4	SSAKA0006UCZZ	AA		D	Vinyl bag (50x60mm)
5	SSAKH0015HCZZ	AA		D	Vinyl bag (180x280mm)
6	SSAKH4001KCZZ	AC		D	Vinyl bag (500x500mm)
7	TCAUS1001ACZZ	AB		D	Caution label
8	TINSE1286ACZZ	AR	N	D	Instruction book
9	TLABZ1025ACZZ	AB		D	Drive No. label

MZ1R25

1 MZ1F19 Exteriors

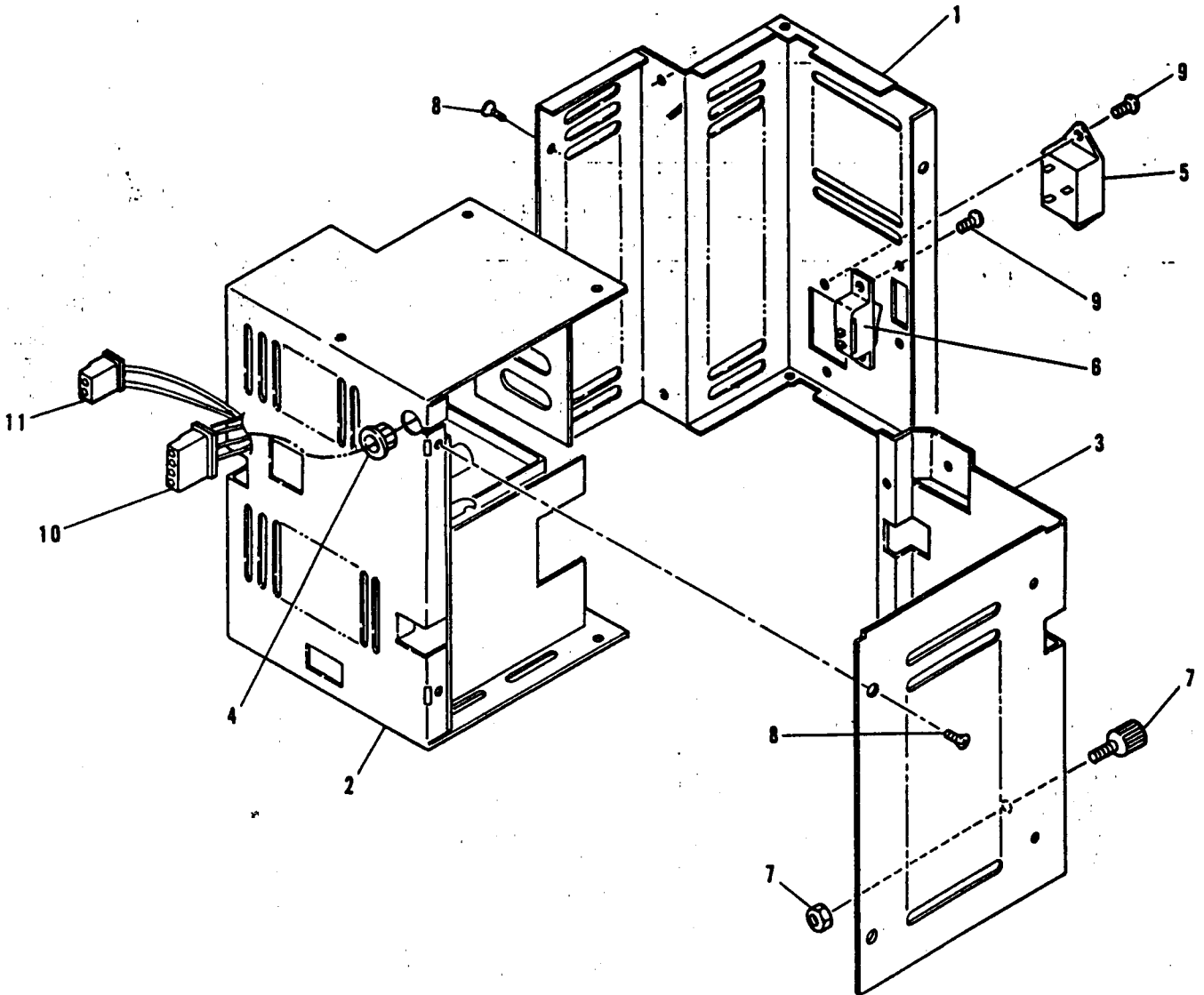


4 Power supply unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	OCF68-5336A//	AM	N	C	Case (Main)
2	OCF68-5337A//	AM	N	C	Case (Sub)
3	OCF68-5338A//	AS	N	C	Panel
4	OCF68-5260A//	AD	N	C	Bushing (OCB-375)
5	OCF68-3584A//	AH	N	C	AC inlet (CM-6)
6	OCF68-4551A//	AP	N	B	Switch (T8220(SB)) (SW1)
7	OCF68-3367A//	AE	N	C	Terminal ass'y (LX-BZ3125CEFN)
8	OCF68-0050H//	AA	N	C	Screw (M3X5)
9	OCF68-5800C//	AA	N	C	Screw (M3X6)
10	OCF68-3582A//	AN	N	C	Connector ass'y (4P) (CN1)
11	OCF68-3583A//	AF	N	C	Connector ass'y (2P) (CN2)
101	OCF68-1122A//	BA	N	B	Power transformer (T1)
102	OCF68-1395A//	AF	N	C	Choke coil (L2,3)
103	OCF68-1380i//	AH	N	C	Coil (SF-T10-40) (L1)
104	OCF68-0028A//	AA	N	C	Fuse holder
105	OCF68-3368A//	AD	N	C	Tab for PWB (61024-1)
106	OCF68-5339B//	AA	N	C	Band (08432)
107	OCF68-4926G//	AC	N	C	Resistor (ERG-2ANJ221) (R2)
108	OCF68-3264A//	AE	N	B	Resistor (EVN-38CA00B23) (VR1,2)
109	OCF68-0353A//	AC	N	C	Wire (Manganese) (R5)
110	OCF68-2650N//	AE	N	C	Capacitor (10ELM1000S) (C7)
111	OCF68-2650T//	AC	N	C	Capacitor (16ELM100S) (C6)
112	OCF68-2650X//	AF	N	C	Capacitor (16ELM1000S) (C2)
113	OCF68-2651T//	AL	N	C	Capacitor (35ELM2200S) (C1)
114	OCF68-2651V//	AB	N	C	Capacitor (50ELM1S) (C9)
115	OCF68-2755M//	AB	N	C	Capacitor (FCQ-M1H103KV) (C4)
116	OCF68-2918Y//	AC	N	C	Capacitor (ECQ-V1H104JZ) (C3,5)
117	VRD-ST2EY561J	AA		C	Carbon resistor (1/4W 560Ω ±5%) (R18)
118	VRD-ST2EY102J	AA		C	Resistor (1/4W 1KΩ ±5%) (R16,17,22)
119	VRD-ST2EY202J	AA		C	Resistor (1/4W 2KΩ ±5%) (R13,15)
120	VRD-ST2EY272J	AA		C	Resistor (1/4W 2.7KΩ ±5%) (R7)
121	VRD-ST2EY103J	AA		C	Resistor (1/4W 10KΩ ±5%) (R6,11)
122	VRD-ST2EY223J	AA		C	Resistor (1/4W 22KΩ ±5%) (R4,21)
123	VRD-ST2EY221J	AA		C	Resistor (1/4W 220Ω ±5%) (R3)
124	VRD-ST2EY472J	AA		C	Resistor (1/4W 4.7KΩ ±5%) (R9,10)
125	VRD-ST2EY104J	AA		C	Resistor (1/4W 100KΩ ±5%) (R12)
126	VRD-ST2HY100J	AB		C	Resistor (1/4W 10Ω ±5%) (R20)
127	VRD-ST2EY224J	AA		C	Resistor (220KΩ)(1/4W) (R14)
128	VRD-ST2EY681J	AA		C	Resistor (R1/4PT681J) (R23)
129	OCF68-2002B//	AB	N	B	Transistor (2SA1015Y) (TR3)
130	OCF68-2004C//	AK	N	B	Transistor (2SA1244Y) (TR1)
131	OCF68-2004B//	AM	N	B	Transistor (2SC3074Y) (TR2)
132	OCF68-2215A//	AK	N	B	Diode (2B4B41-LC2) (REC1)
133	OCF68-0036H//	AE	N	B	Diode (FRA81-004) (D3)
134	OCF68-2303J//	AH	N	B	Diode (ERB84-009) (D1)
135	VHDDS1588L2-1	AB		B	Diode (DS1588L1) (D2)
136	OCF68-1901A//	AM	N	B	IC (MB3759) (IC1)
137	OCF68-1929A//	AH	N	B	IC (UPC393C) (IC2)
138	VRD-ST2EY470J	AA		C	Resistor (47ΩJ 0.25W) (R1)
139	VRD-ST2EY101J	AA		C	Resistor (1/4W 100Ω ±5%) (R19)
140	VRD-ST2EY271J	AA		C	Resistor (1/4W 270Ω ±5%) (R8)
141	OCF68-2760D//	AE	N	C	Capacitor (CFD22B104M) (C8)
142	OCF68-4562H//	AF	N	A	Fuse (EQ315mA)

MZ1R25

4 Power supply unit



5 MZ1E19 Electronic parts

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	VHIM74LS00/-1	AE		B	IC (M74LS00)
2	VHIM74LS02/-1	AE		B	IC (M74LS02)
3	VHIM74LS244-1	AM		A	IC (M74LS244P)
4	VCEAAUIAW107Q	AB		C	Capacitor (10V 100 μ F 6.5 ϕ × 10)
5	VCTYPU1NX104M	AB		A	Capacitor (12WV 0.10 μ F)

6 MZ1E19 Connector & Hardware

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	GFTAT1027ACZZ	AC	N	C	Lid
2	LANGT1076ACZZ	AF		C	Connector fixing angle
3	PSPAF1010ACZZ	AB		C	Spacer
4	PZETV1011ACZZ	AC	N	C	Sheet
5	QCNCM1051ACZZ	AK		C	Connector
6	XBPSD30P06KS0	AA		C	Screw (3×6KS)
7	XUPSD30P08000	AA		C	Screw (3×8)

7 MZ1E19 Packing & Others

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	RMEMR1028AC89	BB		D	Master disk
2	RMEMR1028AC90	BB		D	Utility
3	SPAKA1634ACZZ	AH	N	D	Packing cushion
4	SPAKC1587ACZZ	AK	N	D	Packing case
5	SSAKA0006UCZZ	AA		D	Vinyl bag (50×60mm)
6	SSAKA0302CCZZ	AA		D	Poly Bag(1/F unit) (160×200mm)
7	SSAKB0002YDE0	AA		D	Poly Bag(Media)
8	TINSE1225ACZZ	AQ	N	D	Instruction book
9	TINSE1226ACZZ	AS	N	D	Instruction book
10	TLABE1112ACZZ	AC	N	D	Master label
11	TLABE1113ACZZ	AC	N	D	Utility label
12	TLABM1107ACZZ	AB		D	Model badge
13	TSELF1002ACZZ	AA		D	Label

8 MZ1R18 Electronic parts

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	VHIM74LS00/-1	AE		B	IC (M74LS00)
2	VHIM74LS04/-1	AE		B	IC (M74LS04)
3	VHISN74LS193N	AR		B	IC (SN74LS193N)
4	VHIM74LS257-1	AQ		B	IC (M74LS257P)
5	VHIM74LS30/-1	AE		B	IC (M74LS30P)
6	VHIM74LS367-1	AH		B	IC (M74LS367P)
7	VHIM74LS42/-1	AF		B	IC (M74LS42)
8	VHIM74LS74/-1	AG		A	IC (M74LS74P)
9	VH14164P150-M	AX		B	IC
10	VCTYPU1NX104M	AB		A	Capacitor (12WV 0.10 μ F)
11	VCEAAUIAW107Q	AB		C	Capacitor (10V 100 μ F 6.5 ϕ × 10)

9 MZ1R18 Packing & Others

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	SPAKA1384ACZZ	AH		D	Packing cushion
2	SPAKC1581ACZZ	AM	N	D	Packing case
3	SSAKH1020CCN1	AA		D	Vinyl bag (120×260mm)
4	TINSE1223ACZZ	AK	N	D	Instruction book
5	TSELF1002ACZZ	AA		D	Label
6	PZETV1006ACZZ	AC		D	Insulation sheet

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